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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,242	08/30/2001	Wen Lin	00-LM-117	9379

7590 02/10/2006

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,242	LIN, WEN	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7,10,12,17-22 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,10,12,17-22 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1 – 3, 5, 7, 10, 12, 17 – 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 claims a bus controller that is operable to conduct mass storage transactions between the data memory and the mass storage device. According to Applicant's arguments various prior art bus bridges/controllers identified in the prior rejections are not capable of conducting mass storage transactions, implying that the claimed bus controller plays an active role in conducting the mass storage transaction rather than just being a conduit that provides access paths for such transactions. The specification does not describe any special feature, different from features provided by any other bus/bridge controllers, of the claimed bus controller that enables the bus controller to play an active role in conducting mass storage transactions. The Examiner asks Applicant to specifically point out explain where in the specification the claimed limitation, as argued to be patentably distinct from other bus bridges/controllers, is supported.

All of the claims that depend from claim 1 are rejected for containing the same unsupported limitation as their parent.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites the limitation "the process" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 – 3, 5 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunsaker (US Patent Application Pub. No. 2003/0036198).

7. With respect to claim 1, Hunsaker discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (170) having an interface for communicating mass storage transactions; and

a data memory (system memory 140, alternatively 130 + 140) coupled to and shared by both the processor and the mass storage device (the system memory is shared by the processor via the host bus 120, peripherals via primary bus 195 and other I/O devices including mass storage devices via the ICH 150);

a bus controller (ICH 150) having a memory interface coupled (150 is coupled to 140 via 130) to the data memory and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (150 is coupled directly to 170 without anything in between) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

8. With respect to claim 2, the data memory is coupled to the processor by a memory bus (system memory 140 is coupled to the processor via its own memory bus through the controller 130) operating independent of the data/control bus (the host bus 120 and the unlabeled memory bus are independent buses). The Examiner notes that the only configuration where there are two busses directly coupled to the processor is the one shown in figure 6. However this configuration does not meet the controller requirements of claim 1.

9. With respect to claim 3, the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor (the controller MHC 130 controls access to the system memory and is the nexus that connects all of the claimed elements).

10. With respect to claim 5, the data memory is coupled to the data/control bus (130 is coupled to 120 via 130, or 130 is directly coupled to 120).

11. With respect to claim 21, the mass storage device comprises an optical storage device (CD ROM 172).

12. Claims 1, 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi *et al.* (US Patent No. 6,601,126, hereinafter "Zaidi").

13. With respect to claim 1, Zaidi discloses a computing system (figure 28) comprising:

a processor having a data/control bus interface(CPU or CPU + cache);

a data/control bus (CPU bus or the bus connecting the cache to the bridge) implementing one or more device communication channels;

a mass storage device (DMA peripheral, see col. 27, lines 41 – 45) having an interface for communicating mass storage transactions; and

a data memory (DRAM) coupled to and shared by both the processor and the mass storage device (neither the CPU nor the DMA peripherals have exclusive access to the DRAM memory, the DRAM is shared by all components that has access to it);

a bus controller (bridge and MAC) having a memory interface coupled to the data memory (MAC is coupled to DRAM) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (bridge is coupled to DMA peripherals via a PCI bus without an intermediary controller) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

14. With respect to claim 12, (figure 1, and col. 4, lines 27 – 46, figure 28 is one of the embodiments of this system on chip) the controller is integrated with the processor on a single integrated circuit chip.

15. With respect to claim 20, the computing device comprises a network appliance (col. 27, lines 40 – 45, in a networking application one of the DMA peripherals would be a network controller) having a network controller coupled to the data/control bus.

16. Claims 1, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty *et al.* (US Patent No. 6,128,669, hereinafter "Moriarty").

17. With respect to claims 1 and 14, Moriarty discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (100);

a data/control bus (102) implementing one or more device communication channels;

a mass storage device (118 and 144) having an interface for communicating mass storage transactions;

a data memory (104, or alternatively 112) coupled to and shared by the processor and the mass storage device; and

a bus controller (106, or alternatively 106 and 108) having a memory interface coupled to the data memory (106 is coupled to 104) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (106 is coupled to 120, note that there's no patentable distinction between Applicant's mass storage device, figure 3, 303 + 307, and Moriarty's mass storage device, 120 + 144, they both consist of a controller and a disk) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

18. With respect to claim 20, computing device comprises a network appliance having a network controller coupled to the data/control bus (network controller 128 is coupled to 102 through 106).

19. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellison *et al.* (US Patent Application Pub. No. 2002/0144121, hereinafter "Ellison").

Ellison discloses a computing system (figure 1C) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (170) having an interface for communicating mass storage transactions;

a data memory (system memory 140 or alternatively 130 + 140) coupled to and shared by the processor and the mass storage device; and

a bus controller (ICH 150) having a memory interface coupled to the data memory (150 is coupled to 140 via 130) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (150 is directly coupled to 170 without anything in between) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

The computing system comprises a set-top box including processes for implementing audio/video behaviors in the processor (page 1, paragraph 13).

20. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Houston *et al.* (US Patent No. 6,493,656, hereinafter "Houston").

Houston discloses a computing system (figure 1) comprising:

a processor (100) having a data/control bus interface;

a data/control bus (104) implementing one or more device communication channels;

a mass storage device (118, 121 + 122) having an interface for communicating mass storage transactions;

a data memory (106) coupled to and shared by the processor and the mass storage device; and

a bus controller (102, or 114, or 102 and 114,) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions without an intermediary mass storage controller (102 is directly coupled to 121+122 and 118 is directly coupled to 114) between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands (col. 1, lines 37 – 52);

a servo controller coupled the data memory by the controller and configured to generate the commands to the actuator mechanism (figure 2).

21. With respect to claim 18, the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism (col. 5, lines 27 – 37).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 7, 10 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsakar, Zaiti, Moriarty, or Houston in view of Tanenbaum.

Each of the primary references discloses all of the limitations of claim 1 as discussed above. However, they do not specifically disclose that controller process and application behavior processes are implemented using the processor. Nor do they specifically disclose that the processor implements data structures storing physical geometry information about the mass storage devices. On the other hand, Tanenbaum discloses these (page 92, disk task, page 92, other task, for example, terminal, memory, clock, file system, and user programs, and pages 482 – 484).

It would have been obvious to one of ordinary skill in the art, having the teachings of each of the primary reference cited above and Tanenbaum before him at the time the invention

was made, to use Tanenbaum's teachings in order to actually design and implement an operating system.

24. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsakar in view of Yiu.

Hunsaker discloses all of the limitations of the parent claim as discussed above. However, Hunsaker does not specifically disclose that a mass storage device comprises a magneto-optical storage device. On the other hand, Yiu discloses that a mass storage device suitable for storing large volumes of data in a non-volatile manner includes a magneto-optical device (Yiu, paragraph 35).

It would have been obvious to one of ordinary skill in the art, having the teachings of Hunsaker and Yiu before him at the time the invention was made, to include the use of magneto-optical device teachings in the computer system of Husaker, in order to be able to handle a variety of mass storage devices. It also would have been an obvious matter of design choice to use a well known prior art magneto-optical device, as Applicant has not disclosed that the use of magneto-optical device overcomes problems associated with prior art systems or that it was included for any other reason.

Response to Amendment

25. Claim 1 has been amended and a new claim 32 has been added.

26. All prior rejections have been withdrawn.

Response to Arguments

27. Applicant's arguments regarding the Tanenbaum reference are moot since all prior rejections have been withdrawn.

28. Applicant's arguments regarding the Hunsaker and Ellison references are not persuasive. Applicant states "[t]here is no description in these paragraphs regarding ICH that there is no mass storage controller provided in the mass storage device 170 or that the ICH 150 it is configured to 'conduct mass storage transactions between the data memory and the mass storage device.'" The absence of discussion of there being no mass storage controller does not imply its presence. Moreover, the claim does not require that there be no controller in the mass storage device. The claim merely requires that there be no "intermediate mass storage controller" between the bus controller and the mass storage device interfaces. In fact, Applicant's mass storage device includes a controller (see figure 3, 303). Applicant merely defined a mass storage device to be a combination of a disk drive and its controller. Regarding the "conduct mass storage transaction" limitation, all mass storage transaction between the mass storage devices and the system memory must be conducted through the ICH 150. See also the rejection of claim 1 under 35 U.S.C. 112, first paragraph, discussed above.

Applicant further argues that "neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface." The examiner disagrees. As clearly stated in the rejection ICH 150 interfaces directly with mass storage devices. ICH also directly interfaces with the memory hub controller 130, which is a memory

interface. Applicant has not shown why an interface to a memory controller is not a memory interface.

29. With respect to Applicant's argument regarding the Zaidi reference, Applicant merely alleges without any evidence or well-reasoned logical arguments that certain limitations are not taught. Applicant does not explain why the prior art elements specifically pointed in the rejection as teaching various limitations do not read on the claim language. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

30. With respect to Applicant's argument regarding the Moriarty and Houston references, like the arguments against the Zaiti reference Applicant failed to rebut the rejection with evidence or well-reasoned arguments are convincing. There is nothing the claim language that precludes multiple bus traversals. Applicant must specifically discuss why the detailed mappings of the claimed elements provided in the rejections do not correspond or do not read on the language of the claims to successfully overcome the prima facie case presented above.

31. Applicant's arguments regarding the Yiu reference are moot since all prior rejections have been withdrawn.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
February 3, 2006